A 975 to 1960 MHz, Fast-Locking Fractional-*N* Synthesizer with Adaptive Bandwidth Control and 4/4.5 Prescaler for Digital TV Tuners

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Outline

- Motivation
- Synthesizer Architecture
- Proposed Techniques
  - Adaptive Bandwidth Control
  - Division-Ratio-Based AFC Technique
  - 4/4.5 Prescaler
- Measurement Results
- Conclusions

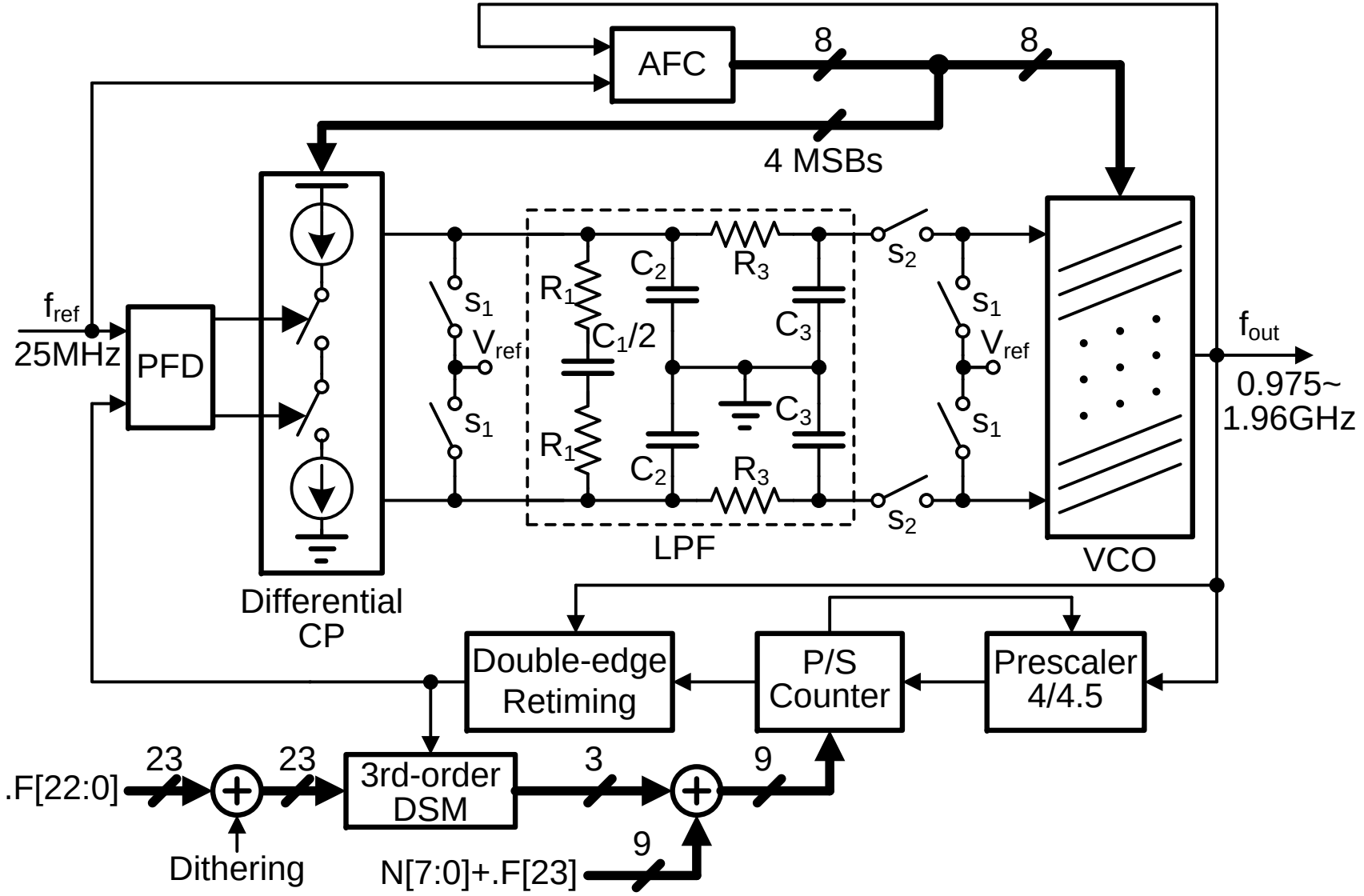
Motivation

- Digital TV tuners need a wideband frequency synthesizer such as DVB-T
- Loop bandwidth changes greatly during a wide frequency range
- Wideband VCO needs AFC to select the sub-band automatically
- Low phase noise and low phase error are required in the receiver

Pros & Cons

- Advantages
  - Loop bandwidth is adaptively controlled
  - Residual fractional error is reduced and VCO clock is counted directly
  - Lower phase noise due to the 4/4.5 prescaler
  - Measured low phase noise, low phase error and fast locking time
- Disadvantages
  - The 4/4.5 prescaler leads to a little bit higher power
  - The fractional spur is high when fractional modulus is close to 0 or 1

Synthesizer Block Diagram



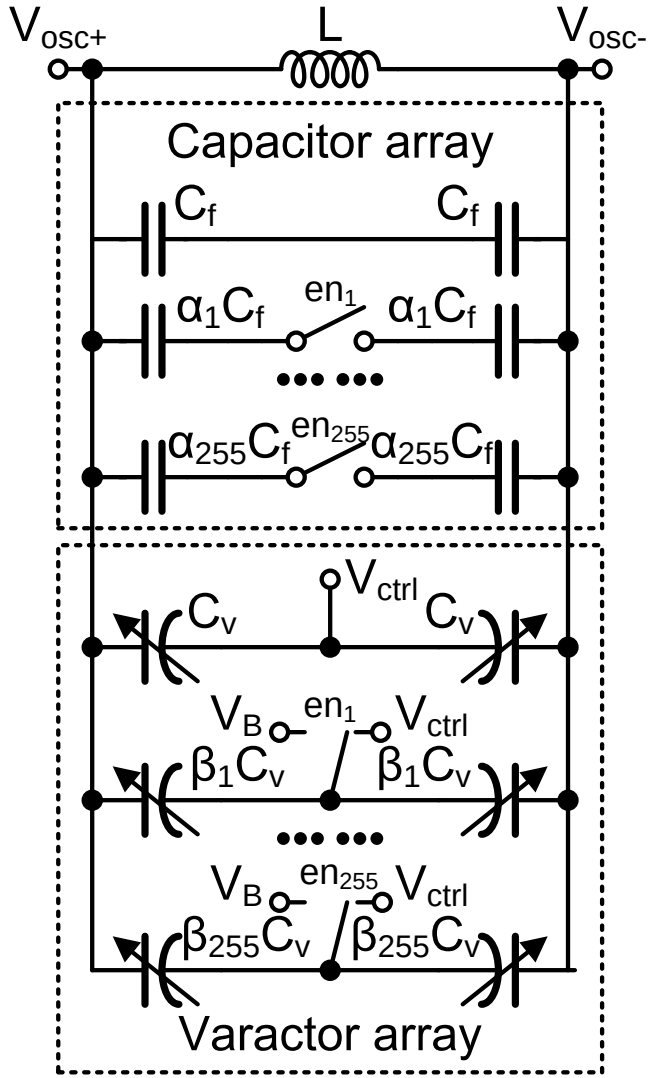
Loop Bandwidth

$$\text{Loop bandwidth} = \frac{I_{\text{CP}} K_{\text{VCO}} f_{\text{ref}}}{2\pi f_{\text{vco}}} \cdot \frac{R_1 C_1}{C_1 + C_2 + C_3}$$

- K_{VCO} and f_{vco} are two factors affecting loop bandwidth
- Maintain loop bandwidth
  - Output frequency f_{vco} varies greatly across the wide range, but I_{CP} also is tuned to compensate f_{vco}
  - K_{VCO} is maintained
  - Then the loop bandwidth is adaptively controlled across the whole frequency range

Simplified *LC*-tank of Multiband VCO

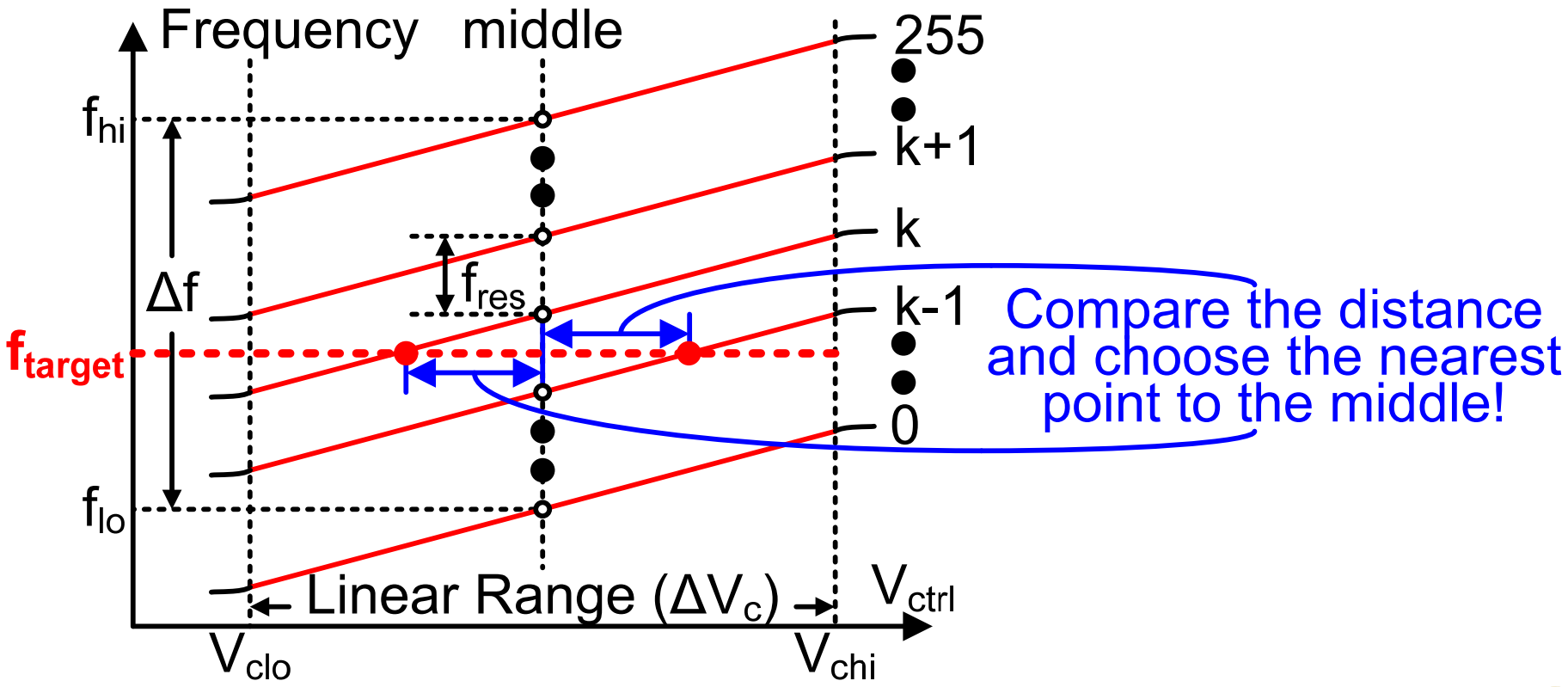
- Switched capacitors and switched varactors are both adjusted simultaneously with different values of units to maintain both K_{VCO} and band steps
- $\alpha_1 \sim \alpha_{255}$ and $\beta_1 \sim \beta_{255}$ are programmed coefficients
- See [Lu, et al., *IEEE RFIC Symp.*, 2008]



Only *LC*-tank depicted

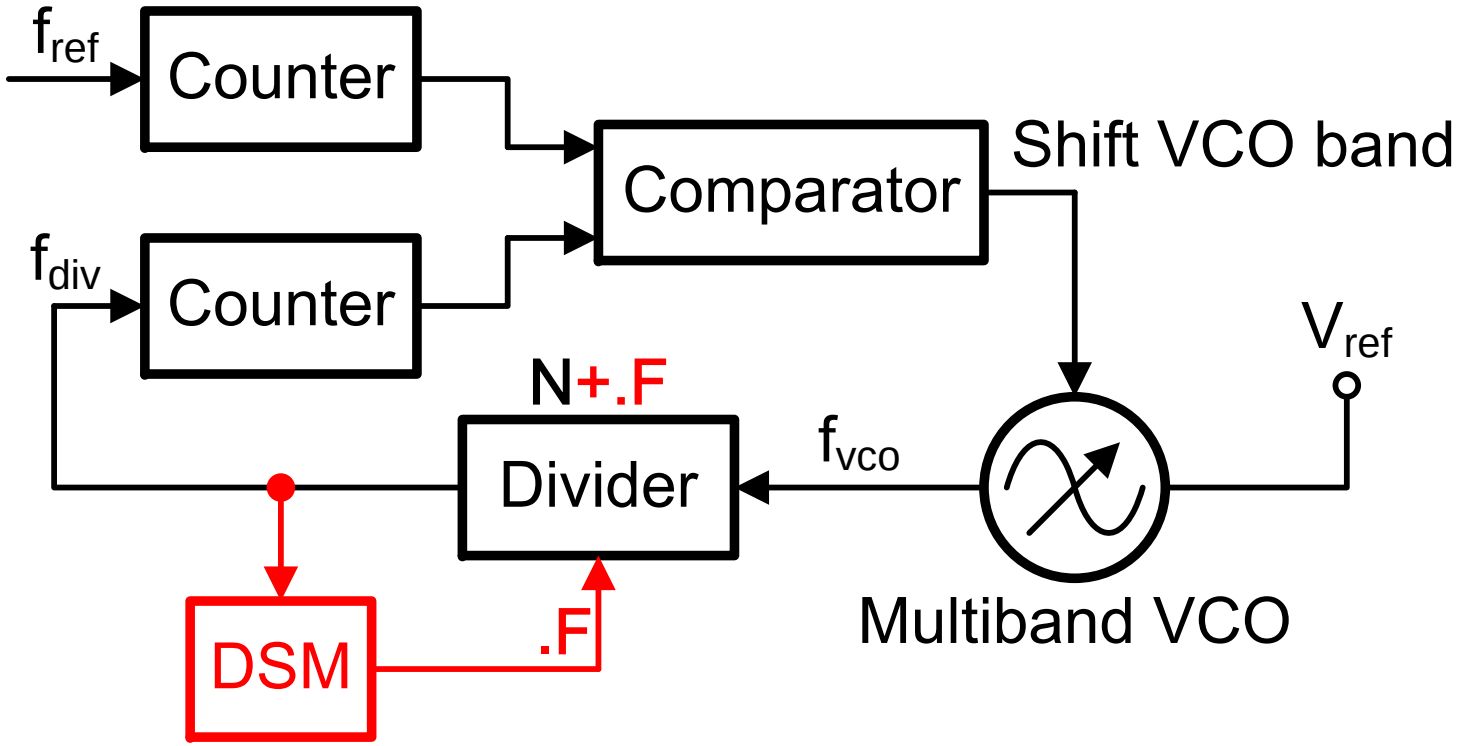
Multiband VCO Calibration Using AFC

- The purpose of AFC is to select the sub-band of VCO whose center frequency is closest to the target frequency automatically

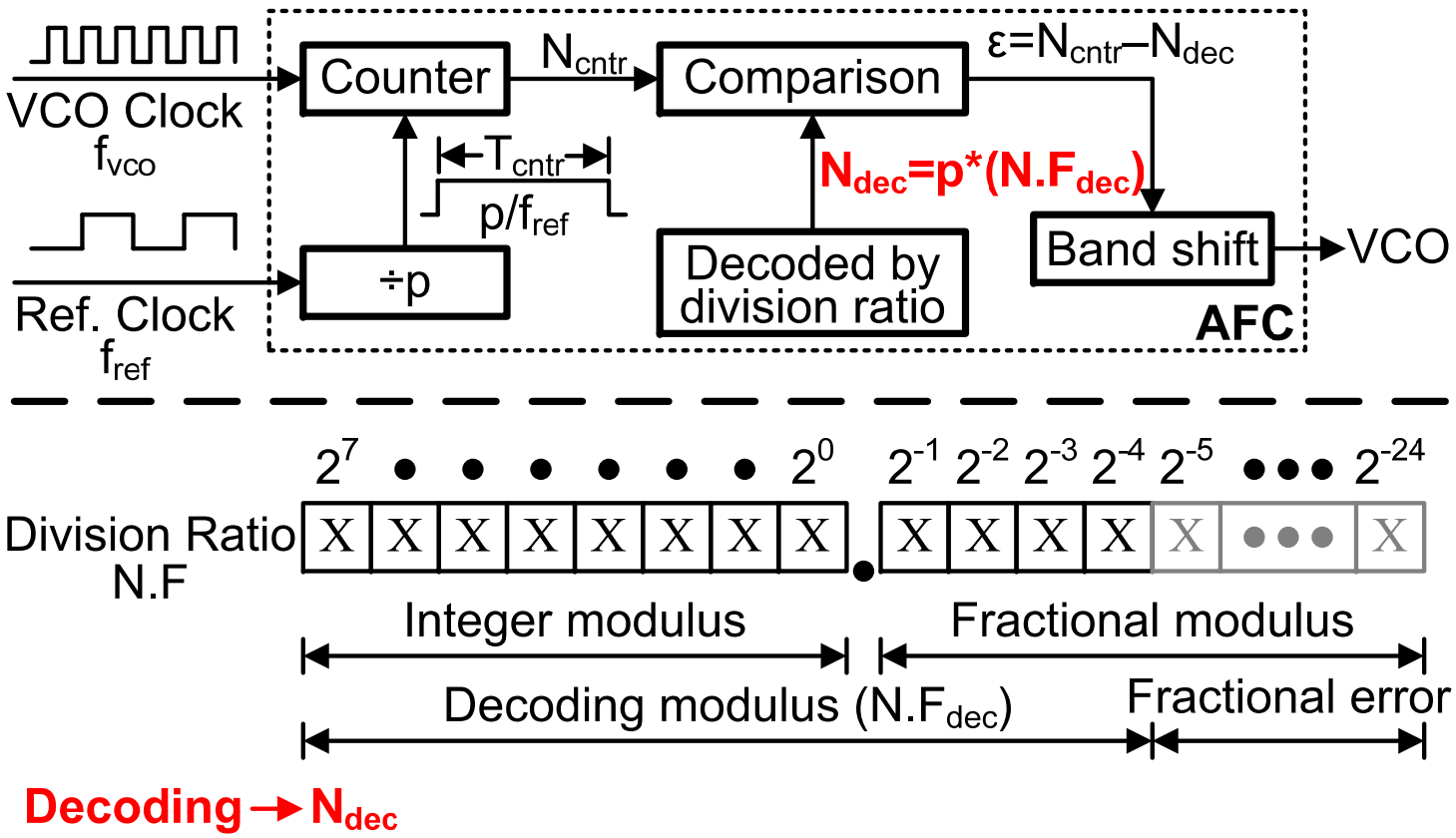


Conventional AFC

- Frequency comparison by counter
- Selected f_{vco} is closest to $N*f_{ref}$, not $(N+.F)*f_{ref}$
  - **Residual fractional error $.F*f_{ref}$ is generated**

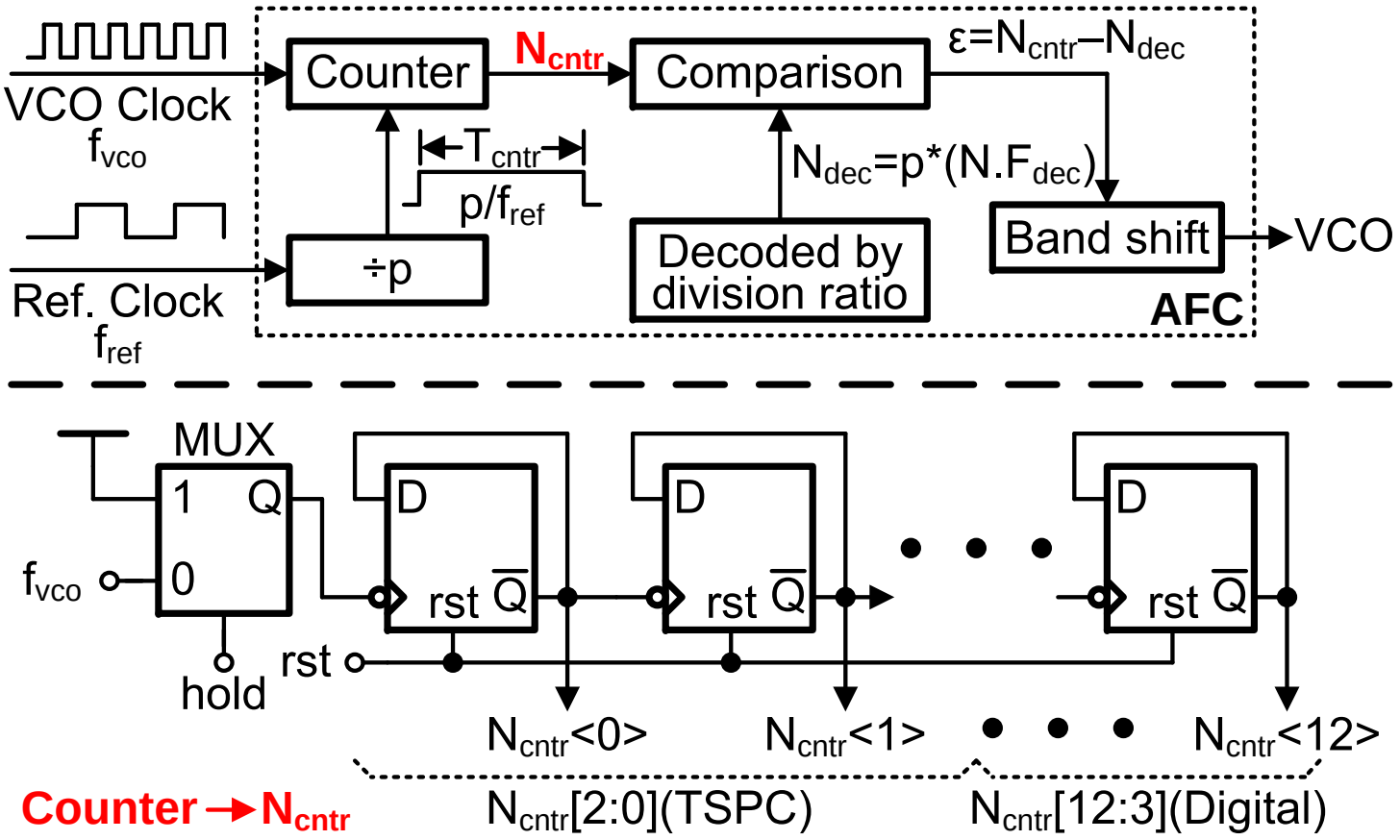


Division-Ratio-Based AFC



- N_{dec} is decoded from the division ratio $N.F_{dec}$,
  - Residual fractional error is reduced to $2^{-4}*f_{ref}$

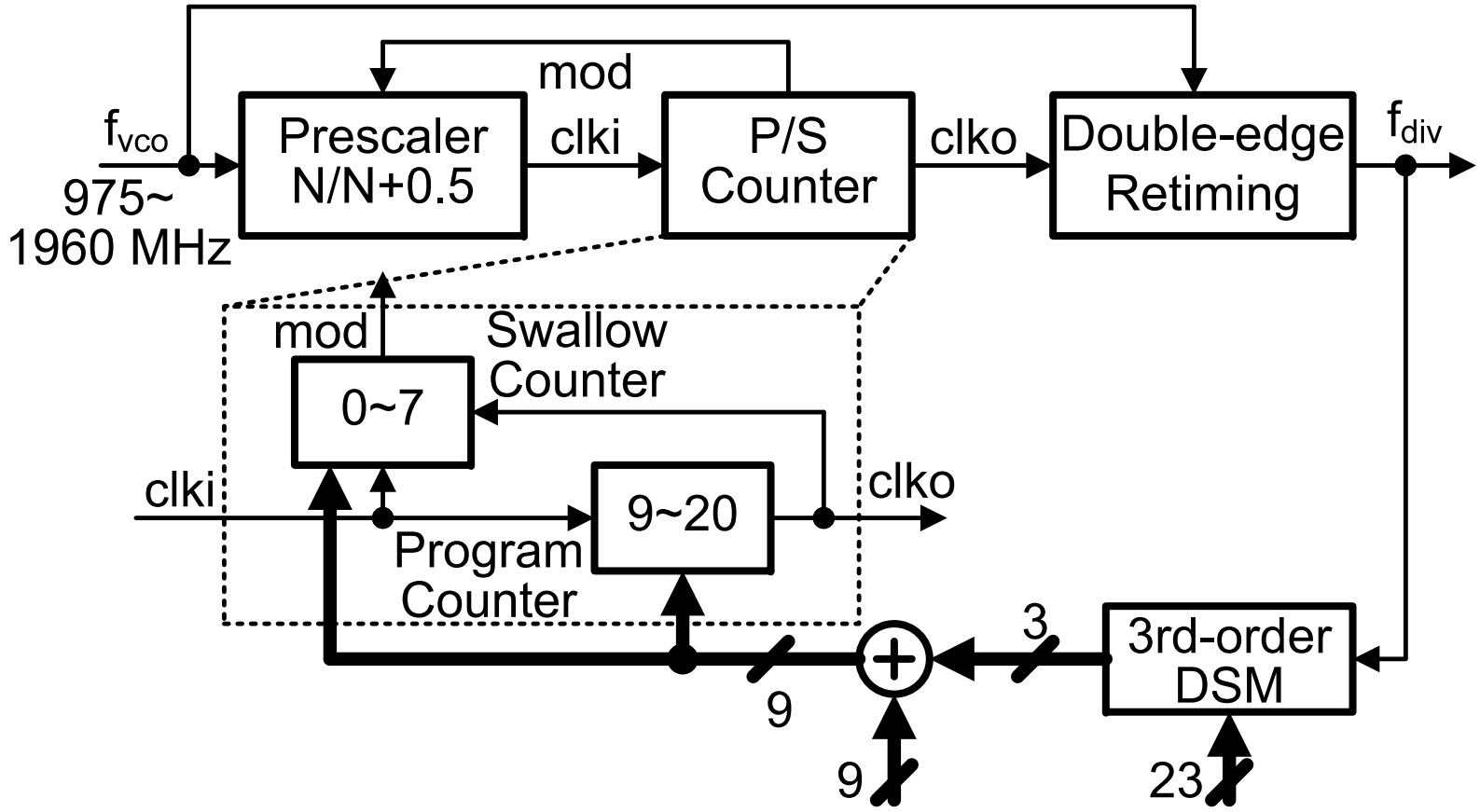
Direct Count of VCO Clock



- High-speed asynchronous divide-by-2 counters are used to count the VCO clock directly

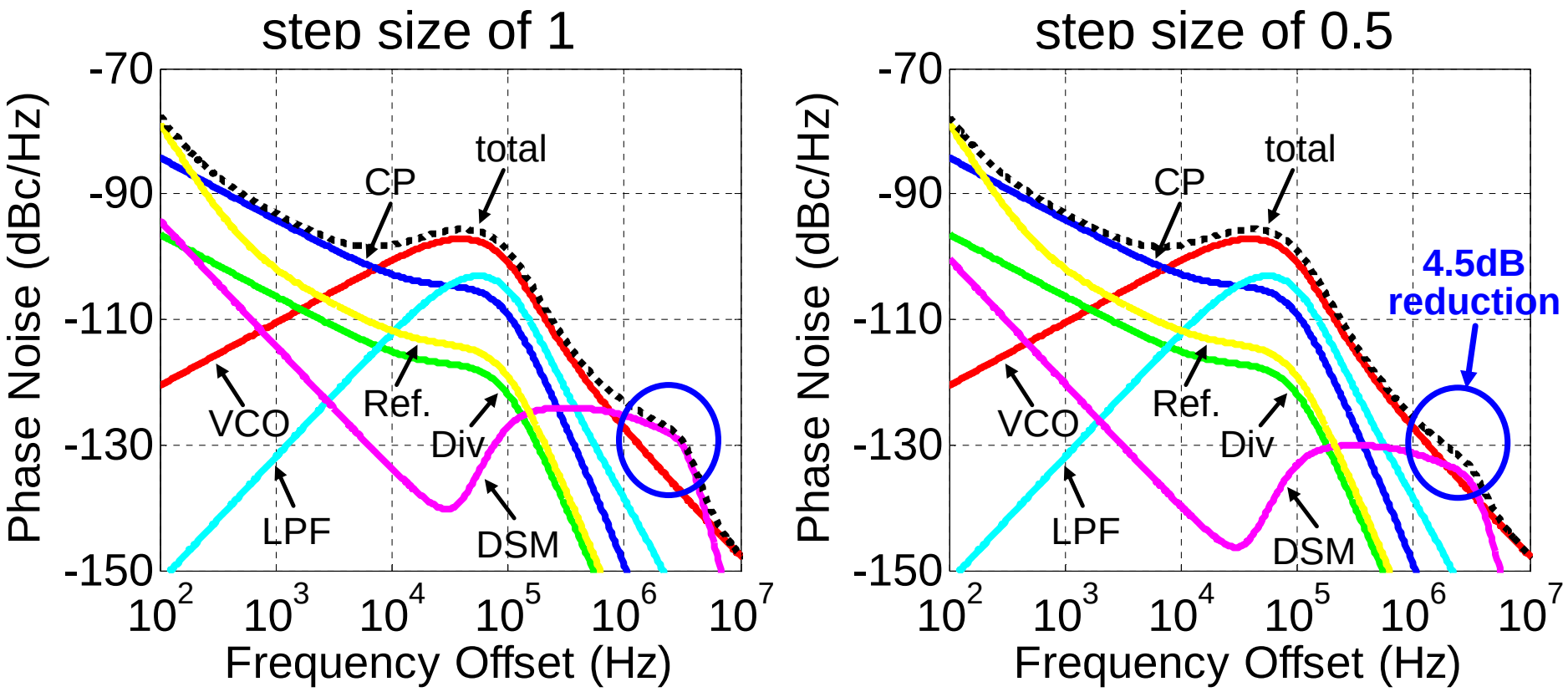
Divider Chain

- *N*=4, *P*=9~20, *S*=0~7, the overall division ratio without DSM is *N***P*+0.5*S=36~83.5 (step=0.5)

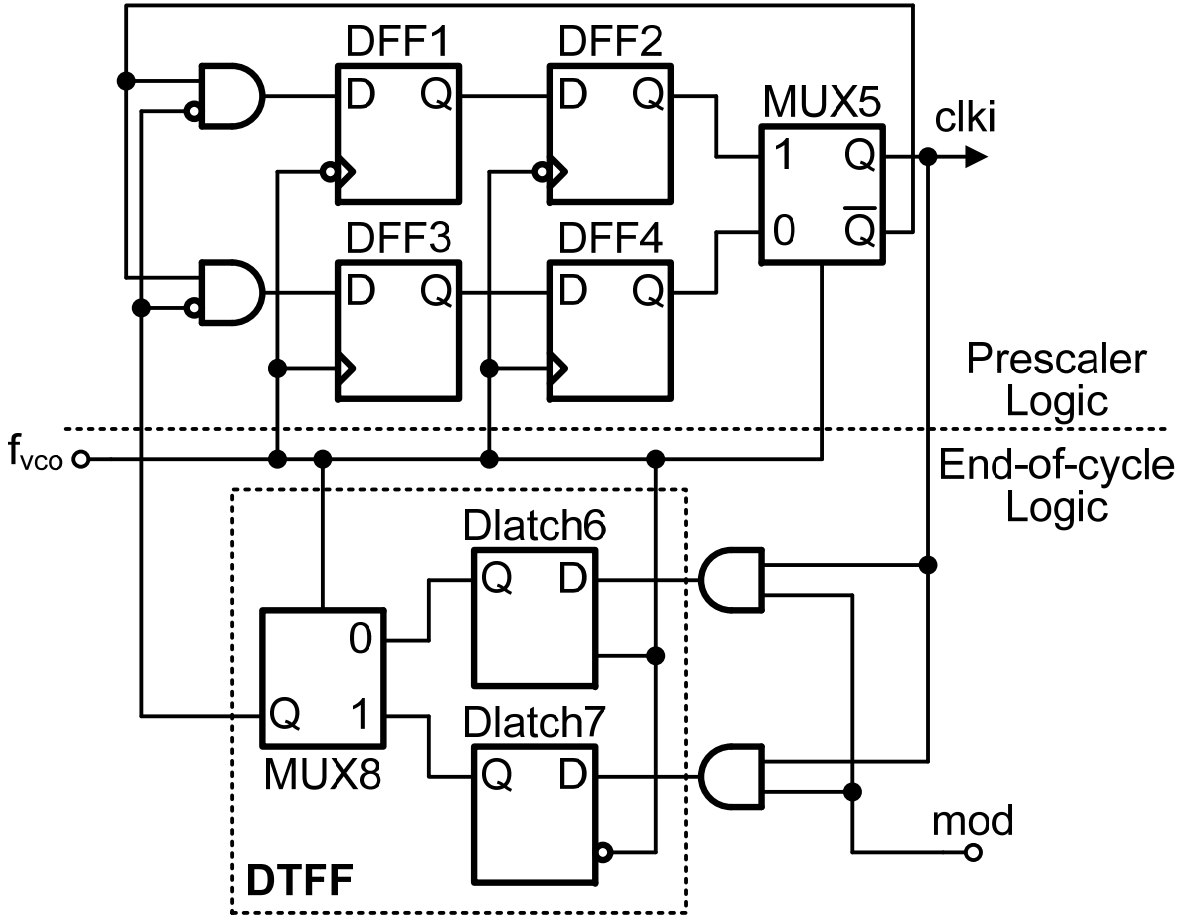


Behavioral Simulations of Phase Noise

- Comparison between step size of 1 and step size of 0.5
- Similar phenomenon in [Yang, et. al., *IEEE JSSC*, Nov. 2006]



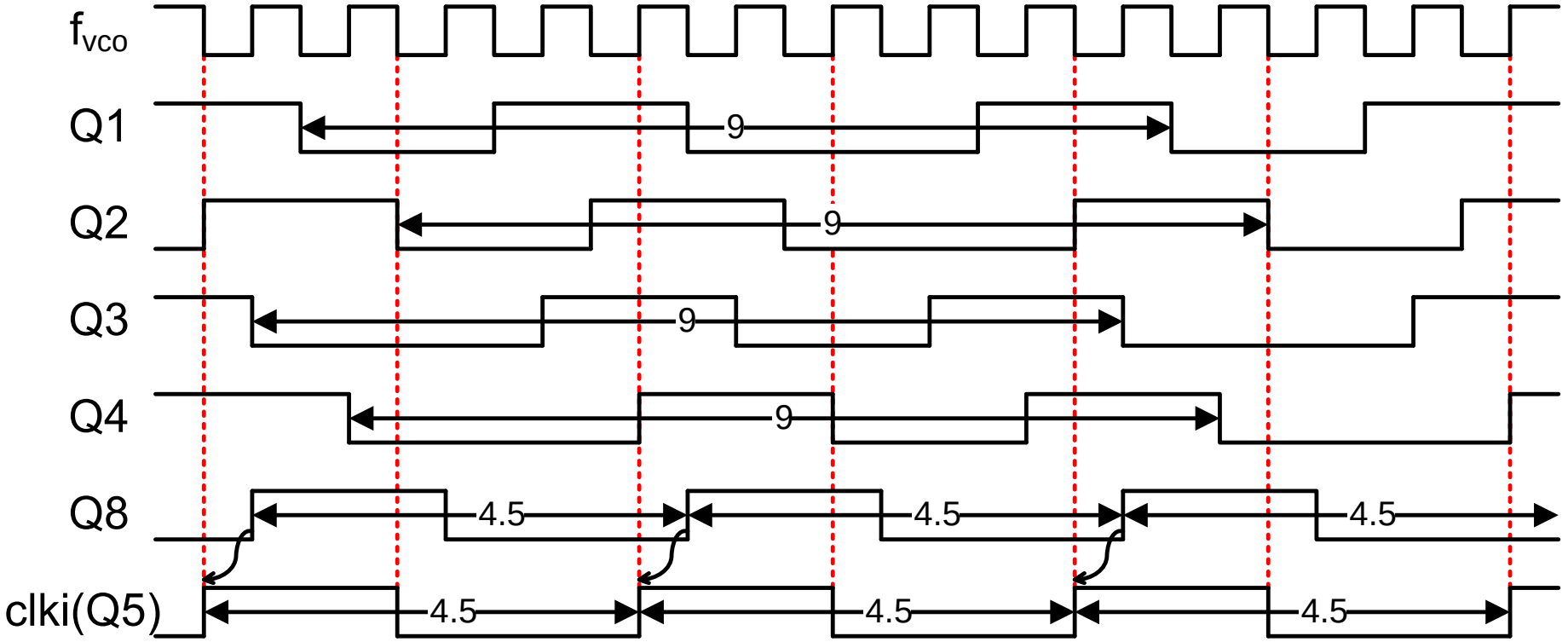
Schematic of 4/4.5 Prescaler



- Works at both rising edge and falling edge
- In divide-by-4.5 mode when mod is high

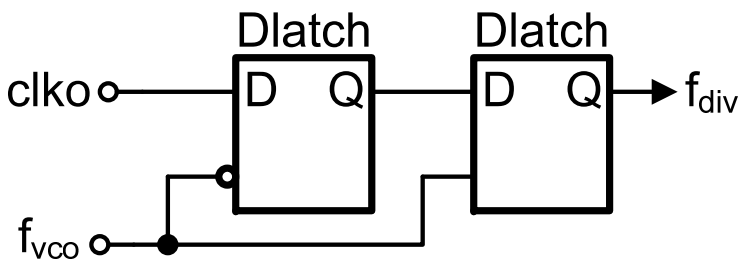
Timing Chart

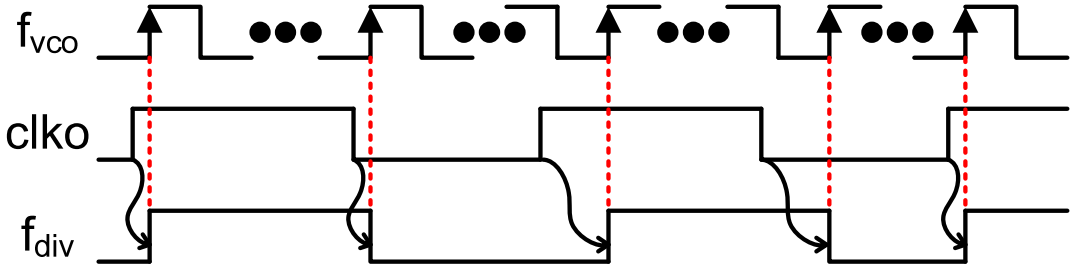
- Divide-by-4.5 mode
- Q8 lags half a period behind Q5



Double-Edge-Triggered Retiming Circuit

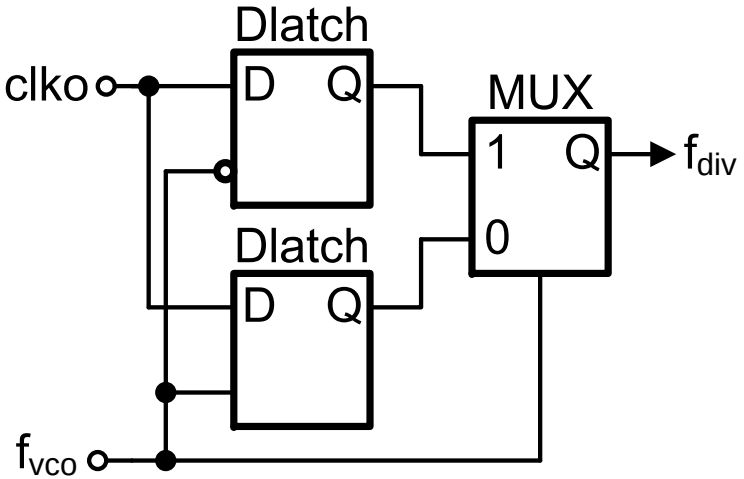
- Comparison between single and double edge
  - ➢ single-edge-triggered retiming

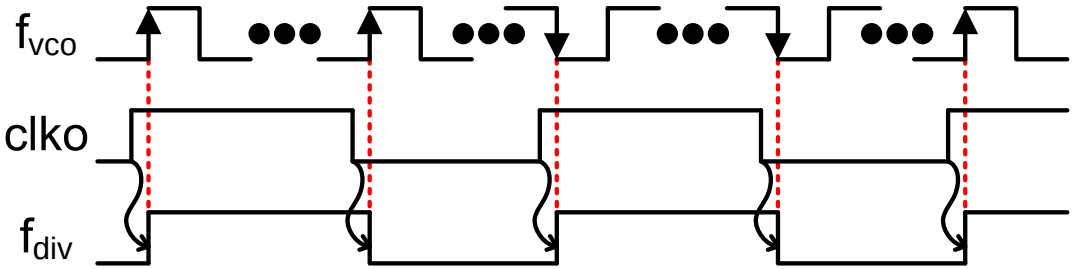




Wrong

  - ➢ double-edge-triggered retiming



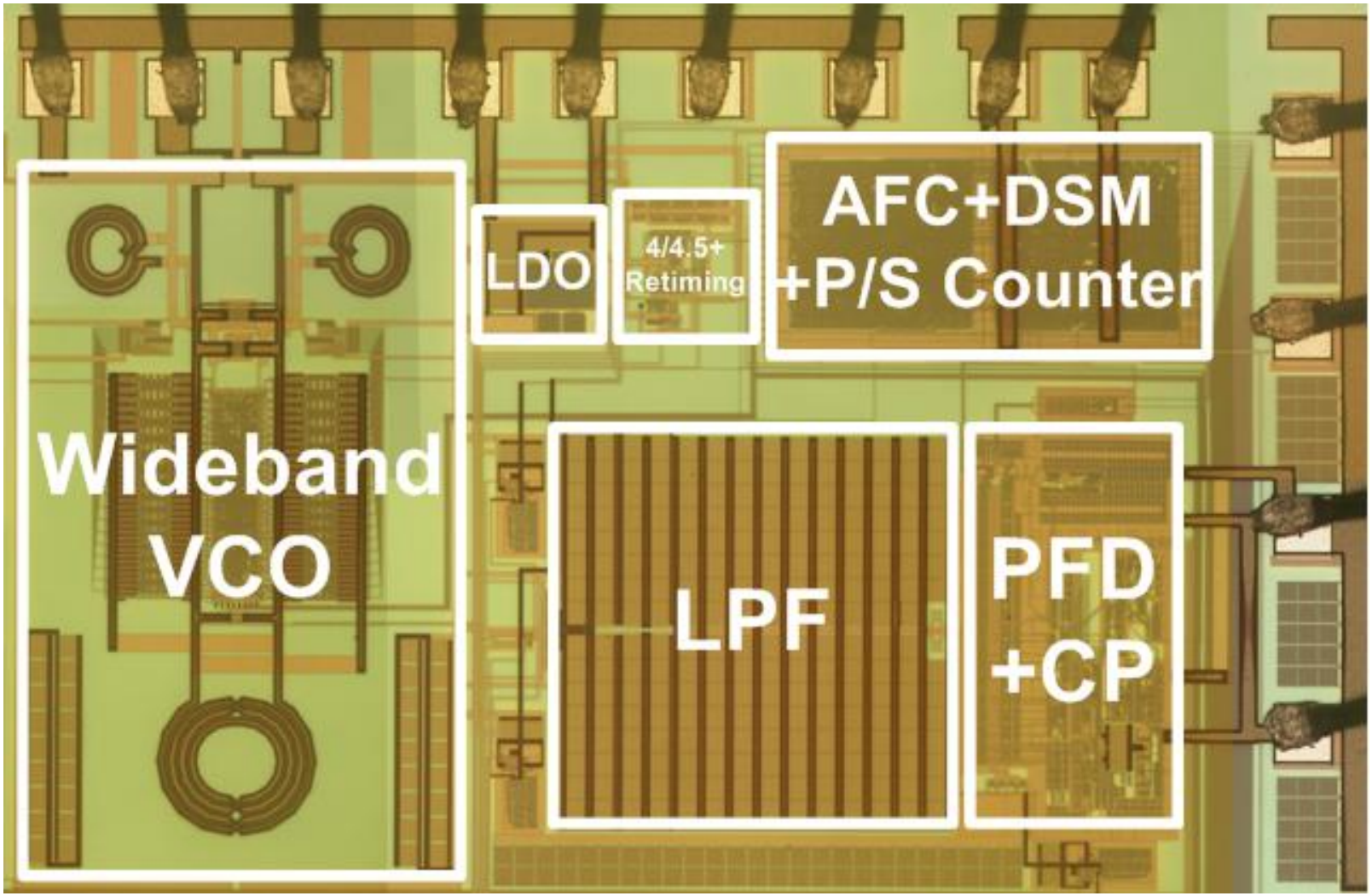


Right

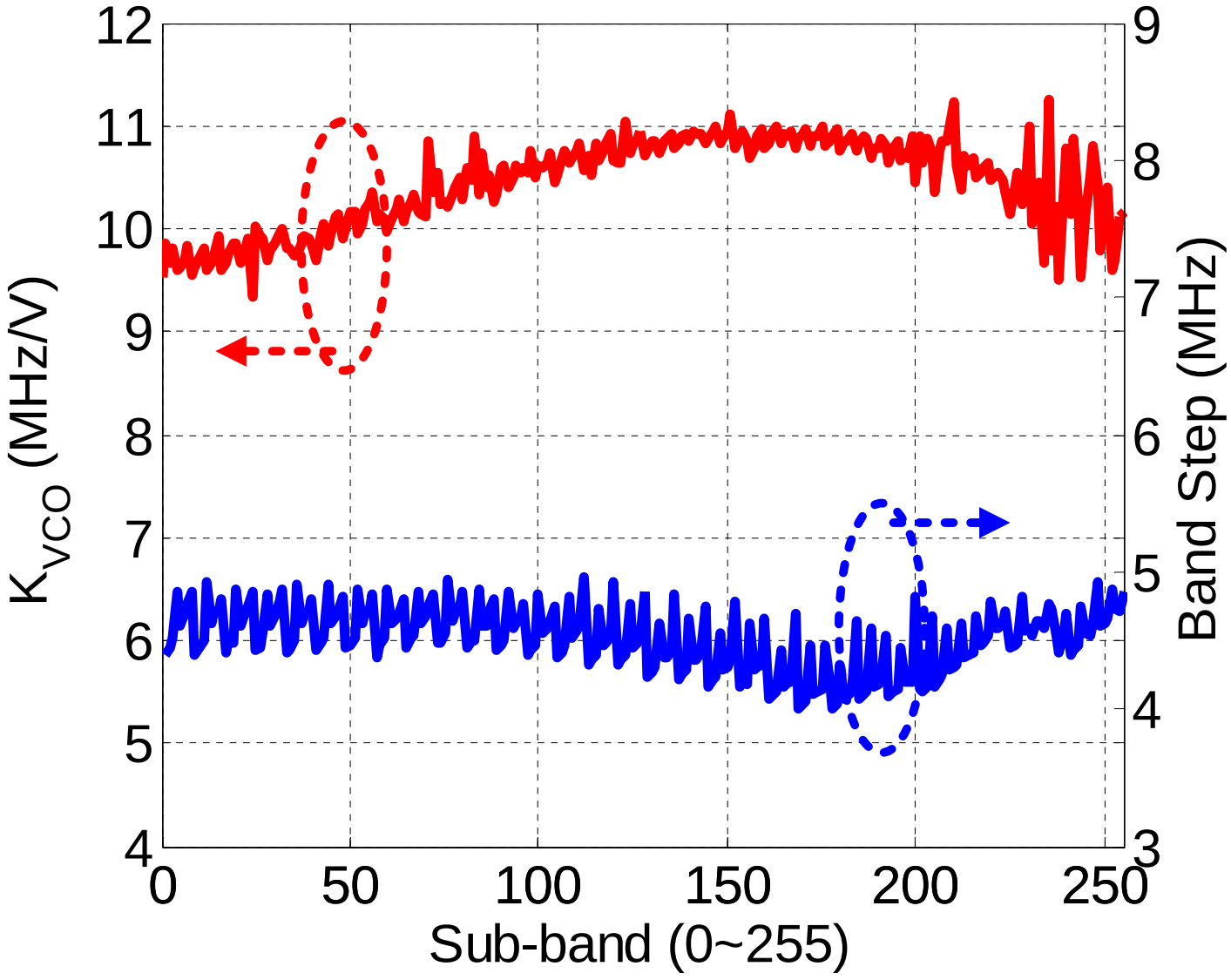
Other Circuit Details

- VCO
  - Power supply from LDO
  - Complementary cross-coupled transistors
  - Two tail inductors to lower the phase noise
- Charge Pump
  - Differentially configured
  - Rail-to-rail CMFB
- Loop Filter
  - On-chip MIM capacitor and high-res poly resistor
- DSM & P/S Counter
  - Programmed using Verilog language

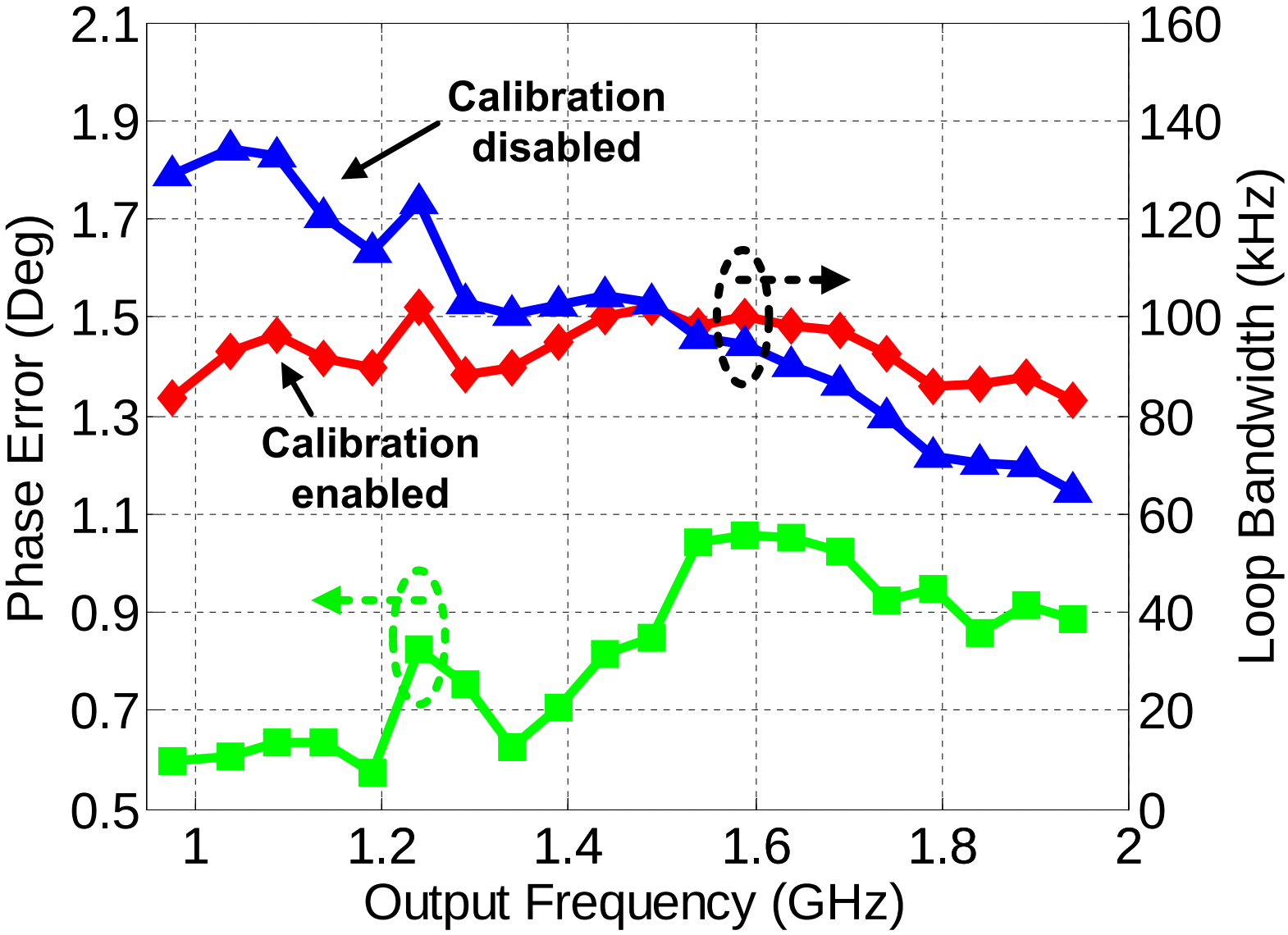
Die Micrograph



VCO Gains and Band Steps

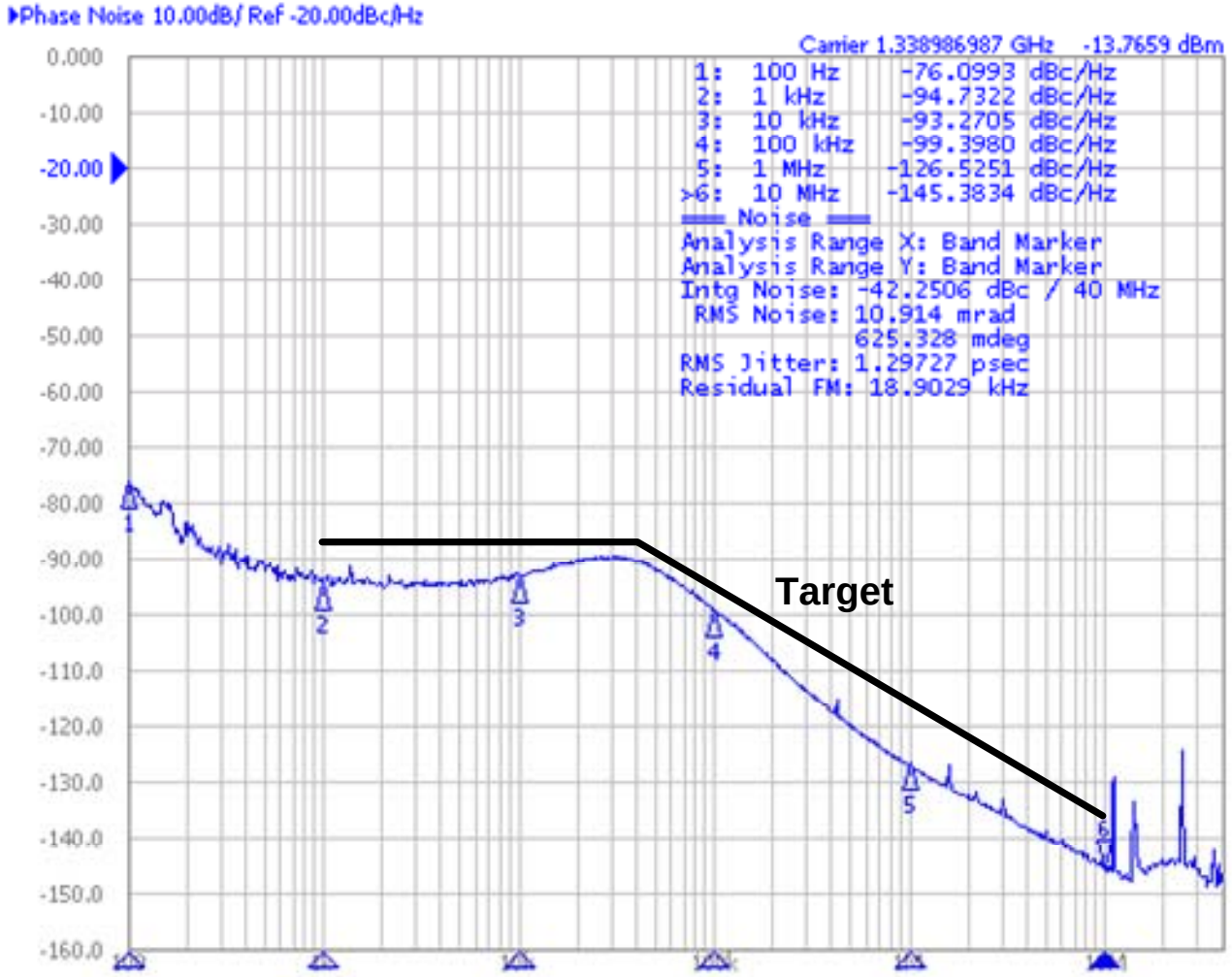


Loop Bandwidth & Phase Error

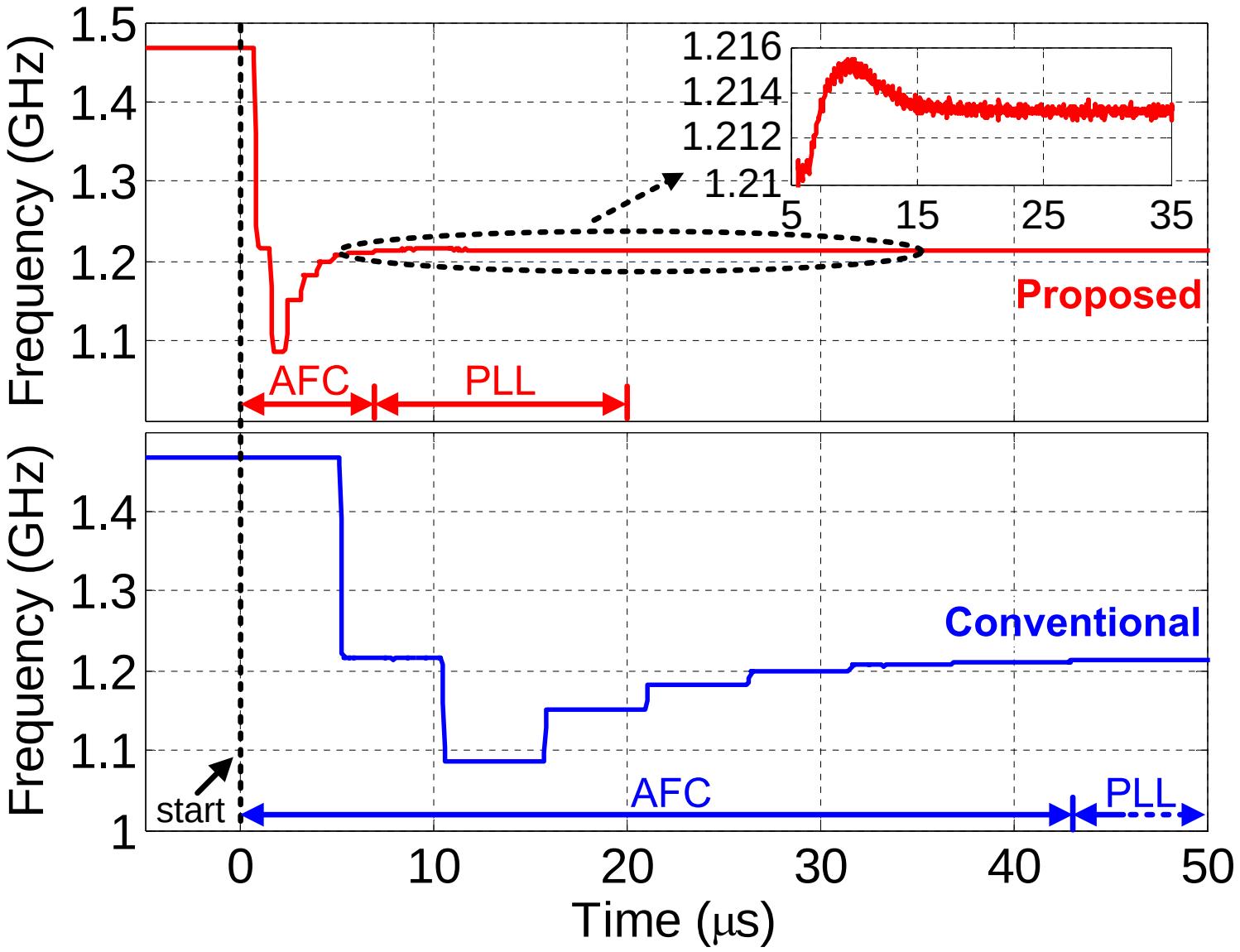


Phase Noise

- The division ratio is 53.56



Locking Time



Performance Summary

Technology	0.18 μm CMOS	Reference Frequency	25 MHz
Die Area	1.58 *1 mm^2	Output Frequency	0.975 to 1.96 GHz (67.1%)
Supply Voltage	1.8 V	Phase Noise (dBc/Hz)	-91@ 3kHz
Current	14 mA		-123@1 MHz
Loop Bandwidth	83 to 102 kHz	Phase Error (rms)	0.6° to 1.05°
Frequency Resolution	< 1.5 Hz	Locking Time	20 μs (6.4 μs for AFC)

Conclusions

- Have demonstrated loop bandwidth is maintained in calibration-enable mode
- Have obtained 20 μs locking time and residual fractional error is reduced for AFC
- Have designed a 4/4.5 prescaler to obtain lower output phase noise contributed from DSM
- Have demonstrated low phase noise and low phase error performance across the whole wideband tuning range